ISSN:0975-9646
Poonam Yadav et al, / (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 2 (4) , 2011, 1750-1752

REDUCTION in POWER DISSIPATION of CPU

Poonam Yadav[1], Surekha Chauhan[2], Madan Shishodia [3]
[1]*ECE Deptt., Jaipur National University,Jaipur INDIA*
[2] *ECE Deptt.Mody Institute of Technology and Science, Rajasthan INDIA*
[3] *CSE Deptt., SUBM, Himachal*

***Abstract*- Power dissipation of the CPU increases drastically with increasing clock frequency and increasing no of transistors. Reducing Power Dissipation of CPU is important for further pushing performance and to avoid increasing cooling cost. In this paper the comparative analysis of various comparator circuit design of ALU is presented to reduce Power dissipation of CPU [1]. Three Comparator circuits chosen for comparison are: Traditional comparator, Domino Style comparator and PLSSC. Though all the circuit will perform the function of a comparator but we have to choose the circuit which has minimum power dissipation.**

Keywords- Power Dissipation, Comparator, Spice

I.INTRODUCTION

Power dissipation is a factor which hinders the overall efficiency of the system. It is basically the power which is converted to heat and to be radiated away from the device for the normal functioning of the device. Electrical devices can handle a certain amount of current for instance a transistor may handle a limited amount of current. This is because of the reason that if they are allowed to handle current beyond this they get too hot and hence can't give full efficiency.

Efficiency ∞ 1/Power dissipation

So Efficiency and power dissipation have an inverse relation and hence Power dissipation reduces efficiency of all the circuits Power dissipation is basically wasted power to keep the device quiescent and operational.

II.POWER DISSIPATION IN CPU

CPU power dissipation is the process in which CPU consumes electrical energy and dissipates this energy both by action of the switching devices contained in CPU and energy is lost in form of heat due to the impedance of the electronic circuits. CPUs typically use a significant portion of the power consumed by the computer. For a given device, operating at a higher clock rate always requires more power. Reducing the clock rate of the microprocessor through power management when possible reduces energy consumption. New features generally require more transistors, each of which uses power. Turning unused areas off saves energy, such as through clock gating. As a processor model's design matures, smaller transistors, lower-voltage structures, and design experience may reduce energy consumption.

A. PROPOSED IDEA FOR REDUCTION OF POWER DISSIPATION IN CPU

Power dissipation in CPU can be reduced in case we consider the complete internal architecture of CPU and then reduce its power dissipation in different parts. As we can easily analyze that CPU have two main units: CU (Control Unit) and ALU (Arithmetic and logic unit).In case we are able to reduce power dissipation in any of the above two we can reduce the overall power dissipation for CPU. In this paper we consider ALU as our device in which we will reduce the power dissipation and hence the overall power dissipation for CPU will be reduced.

B. ALU (Arithmetic and logic unit)

ALU is the main functional unit of CPU. It is the device which is responsible for all the arithmetic and logical operations in CPU. So ALU is the most important part of CPU which can be used as a tool to reduce the power dissipation in device. The figure given below shows the internal architecture of ALU. In ALU as we know we have four blocks. The Add/Sub block[2], Comparator block, Logical unit block and Shift/rotate block. The four blocks performs the functions as required [3]. For example, if we want to perform comparison operation then it is performed with the help of Comparator block.

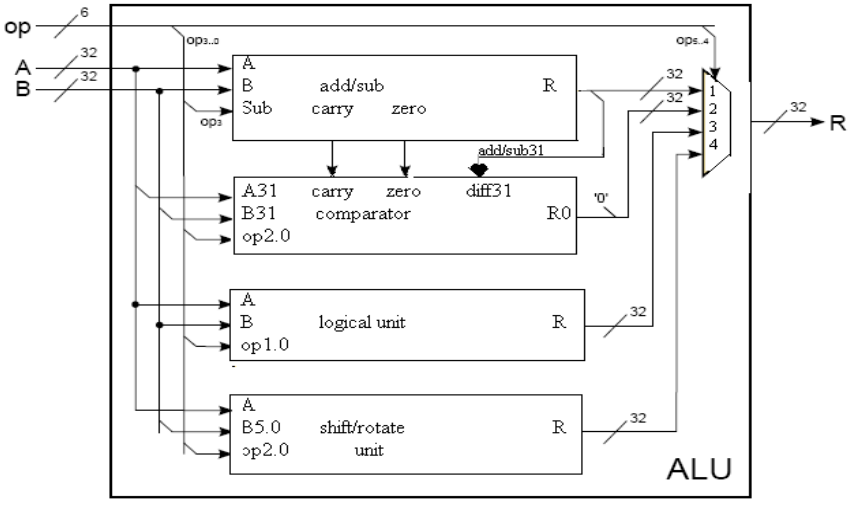

fig1: Internal Architecture of ALU

C. COMPARATOR

The comparator block performs equal, not equal and signed or unsigned, greater or equal and less than comparisons [4].

TABLE1: OPERATION OF COMPARATOR

Operation	Opcode	Logical Function
$A \geq B$ (signed)	001	$(\overline{A_{31}}.B_{31}) + \overline{diff_{31}}.(\overline{A_{31}} \oplus B_{31})$
$A < B$ (signed)	010	$(A_{31}.\overline{B_{31}}) + diff_{31}.(\overline{A_{31}} \oplus B_{31})$
$A \neq B$	011	$\overline{zero}$
$A = B$	100	$zero$
$A \geq B$ (unsigned)	101	$carry$
$A < B$ (unsigned)	110	$\overline{carry}$

To get all these tasks accomplished we have to design a circuit which can perform the functioning given in above table. We can implement this with three styles:

1). Traditional 8 bit Pull Down Comparator: The traditional comparator circuit (also known as a pull–down comparator), dissipates energy on a mismatch in the input arguments (comparands). The output is precharged, and pulled down on a mismatch in any bit position during the evaluation phase, causing energy dissipation [5]. Fig 2 shows 8-bit pull down comparator Effective output loading of traditional comparators is high this is equal to the diffusion capacitances of 2C n–transistors plus the load capacitance, where C is the number of bits compared. This results in considerable power dissipation in the case of a mismatch.

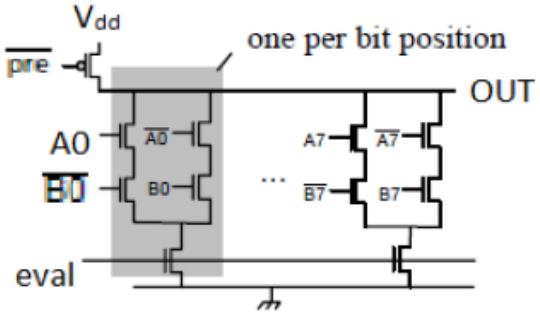

fig2: 8 bit Pull down comparator

Effective output loading of traditional comparators is high this is equal to the diffusion capacitances of 2C n–transistors plus the load capacitance, where C is the number of bits compared. This results in considerable power dissipation in the case of a mismatch.

2). *Two Stage Domino style Comparator*: The circuit shown in Fig. 3 compares two 8 bit comparands using a combination of domino- style logic and pass transistor logic. P-transistor pass logic blocks compare two bits of the comparands at a time. A high voltage is passed on to the right of each transistor block. The precharging signal is cut off during the evaluation phase and an evaluation signal is applied to each stage of the domino logic. The first domino stage pulls down the output of the first stage during the evaluation phase only if the pass transistor logic using p devices (greyed box, P) driving the gates of Q1 and Q2 are both on.

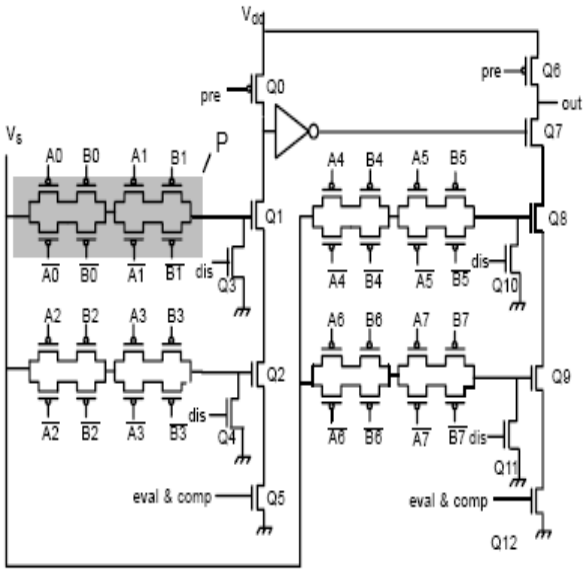

fig3: Two Stage Domino Style Comparator

This happens when all 4 least significant bits are equal. The n-transistors Q3 and Q4 prevent false matches caused by the charge accumulations in previous cycles. During precharging [6], these transistors turn on (this is high) for a small time to discharge the charge stored in the previous cycle (which happens when the corresponding block matches) on the gates of transistors Q1 and Q2. The output of the comparator is discharged to ground only when all bits of the comparands match. To reduce the charge stored at the gates of transistors Q1, Q2, Q8 and Q9 and hence, the energy dissipated when these gates are discharged, a voltage lower than Vdd can be used as Vs. On the flip side, this increases the circuit delay on a match and complicates the design because the additional voltage source has to be provided (which can be either derived On the flip side, this increases the circuit delay on a match and complicates the design because the additional voltage source has to be provided (which can be either derived from the outside of the chip or generated locally from the Vdd).

3). A Pass Logic based Single-Stage Comparator: The Pass Transistor logic passes a high logic level to the gate of the n-transistor Q1 when bits A7 and B7, as well as bits A6 and B6 of the comparands match. The series pull down structure consisting of the devices Q1, Q2, Q3 and Q4 thus conducts when all 8 bits of the comparands are equal. The output of this comparator, precharged to Vdd by Q0 is thus discharged when all bits of the comparands are equal and when the evaluate device, Q5, is on. The n-transistors Q6, Q7, Q8 andQ9 discharge any accumulated charges when partial matches occur [7]. The effective loading of the output is small: the diffusion capacitances of a small p transistor (Q0) and an n-transistor (Q1), plus the gate capacitances of whatever is driven by the output and wire capacitances. As in the case of the domino-style comparator, a lower voltage than Vdd can be used to pass the high voltage level to the gates of n devices.

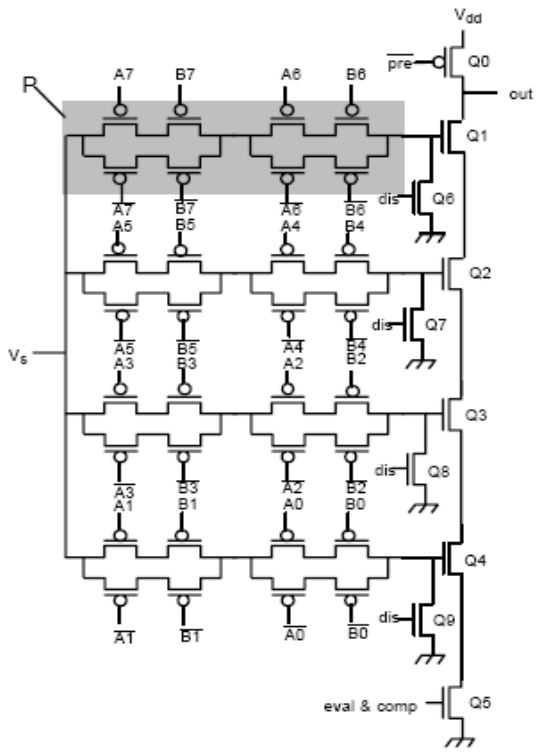

fig4: Pass Logic Based Single Stage Comparator

4). Variation of Energy Dissipation with Vs: The variation of the average energy with the supply voltage for domino, traditional and PLSSC comparators is shown in Fig. 5

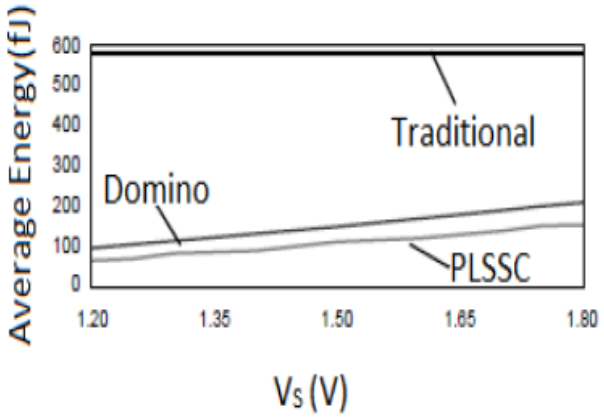

fig5: *Variation of average energy versus Vs*

III.CONCLUSION

Power dissipation has become a major factor in improvement of efficiency of the devices. Since now a days when we are proceeding towards VLSI and ULSI industry there is a major requirement to reduce the power dissipation. In this paper we introduced the design of comparator circuit including PLSSC that has lower power dissipation than the traditional designs .since this factor can hinder the growth and miniaturization of devices. So this logic can further be applied to all other devices and hence we can easily reduce power dissipation substantially in all the circuits.

IV.FUTURE WORK

As said earlier that power dissipation is a major hazard in our industry nowadays so we have to exploit all out techniques so that it doesn't hinders the future growth. So the basic requirement is to implement the logics to different circuits so that power is reduced substantially in all the devices. Power dissipation factor becomes more disaster when we are dealing with the VLSI industry. So necessary steps must be taken in order to avoid the breakdown of devices due to higher power dissipation. Moreover power dissipation factor may be a stepping stone for the development towards miniaturization of all the devices available. Portability of devices can only be achieved with miniaturization, which in turn can only be achieved by reducing power dissipation.

REFERENCES

[1] [Beni94] Benini, L., Favalli, M., and Ricco, B., "*Analysis of Hazard Contributions to Power Dissipation in CMOS ICs." 1994 International* Workshop on Low Power Design, NAPA Valley, April 1994

[2] *[Kilb59] Kilburn, T., Edwards, D.B.G., and Aspinall, D.,* "Parallel addition in DigitalComputers: A New Fast "Carry" Circuit" IEE Proc 106, Pt B 464-466

[3] Emer, J. EV8: *The post–ultimate Alpha. Keynote at International* Conference on PACT, Sep. 2001.

[4] [Skla60] Sklansky, J, "Conditional-Sum Addition Logic.", *IRE Trans on Electronic Computers, EC-9; pp 226-231.*

[5] Ergin, O., Ghose, K., Kucuk, G., Ponomarev, D., *"A Circuit–*

Level Implementation of Fast, Energy–Efficient CMOS Comparators for High–Performance Microprocessors", in Proc. of

ICCD, 2002, pp.118–121.

[6] Kucuk, G., Ghose, K., Ponomarev, D. and Kogge, P.,"Energy–Efficient Instruction Dispatch Buffer Design for Superscalar Processors," in *Proc. ISLPED*, 2001, pp. 237–242.

[7] Palacharla, S., Jouppi, N. P. and Smith, J.E., *"Quantifying the complexity of superscalar processors", Technical report* CS–TR–96–1308, Dept. of CS, Univ. of Wisconsin, 1996.